and an input transistor connected in parallel with the transistor stack, each transistor stack including a first series transistor connected to the second potential, and a second series transistor connected between the first series transistor and one of the output nodes, the first series transistor being larger than the second series transistor.

6. (Amended) The logic stage of claim 21 wherein the second series transistor is to receive a generate input corresponding to a less significant bit, the first series transistor and input transistor to receive inputs corresponding to a more significant bit.

8. (Amended) The logic stage of claim 1 wherein the evaluate circuits include PMOS transistors.

10. (Amended) The logic stage of claim 1 wherein the evaluate circuits include NMOS transistors.

Please add new claim 21 as follows:

21. (New) A logic stage comprising:

a precharge circuit connected to a first potential and a differential output defined by a first output node and a second output node;

a first evaluate circuit connected to a second potential and the first output node; and

a second evaluate circuit connected to the second potential and the second output node, the second evaluate circuit being symmetric with the first evaluate circuit, each evaluate circuit including a transistor stack connected between the second potential and one of the output nodes, and an input transistor connected in parallel with the transistor stack, each transistor stack including a first series transistor connected to the second potential, and a second series transistor connected between the first series transistor and one of the output nodes, the second series transistor to receive a signal that is located in a path that is more critical than a path including a signal received by the first series transistor.